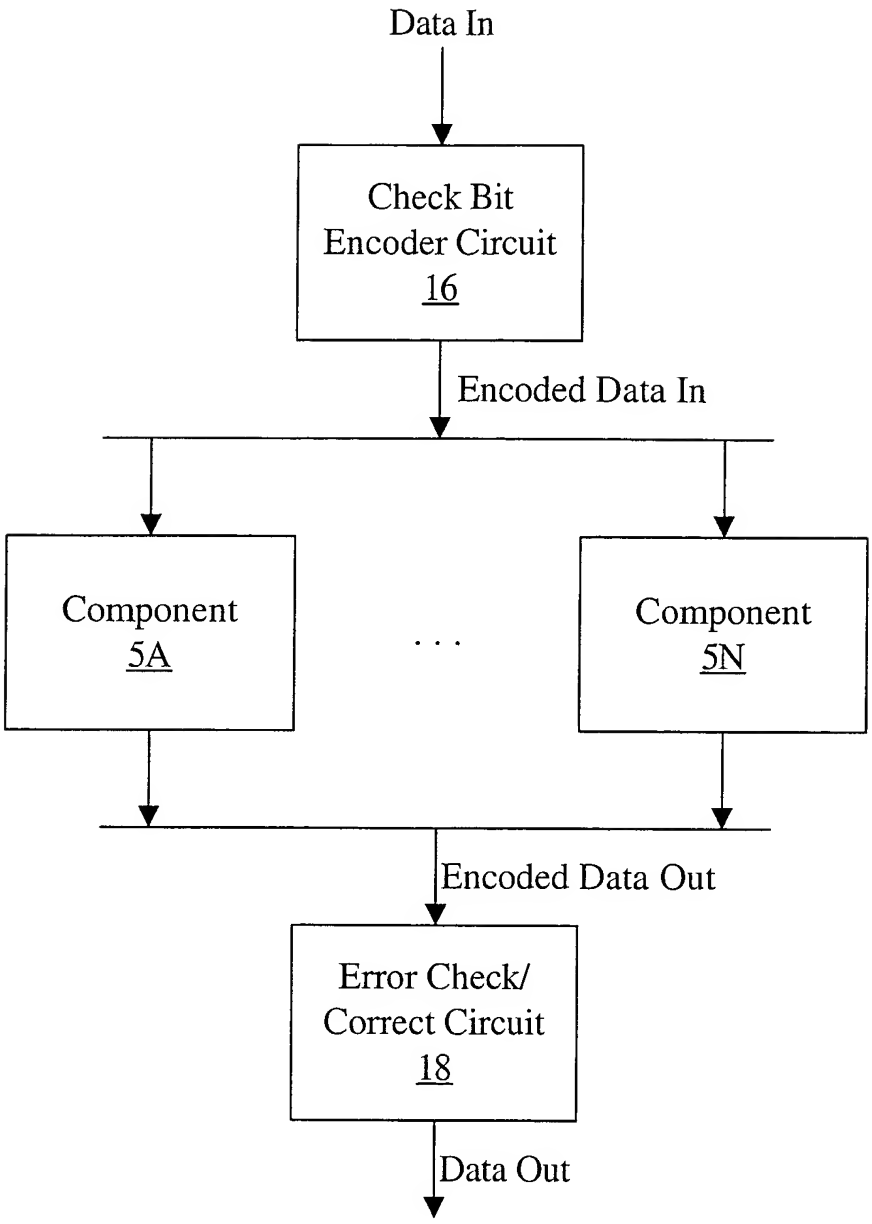
Data In
Check Bit
Encoder Circuit
16
Encoded Data In
Component
5A
. . .
Component
5N
Encoded Data Out
Error Check/
Correct Circuit
18
Data Out

Fig. 1

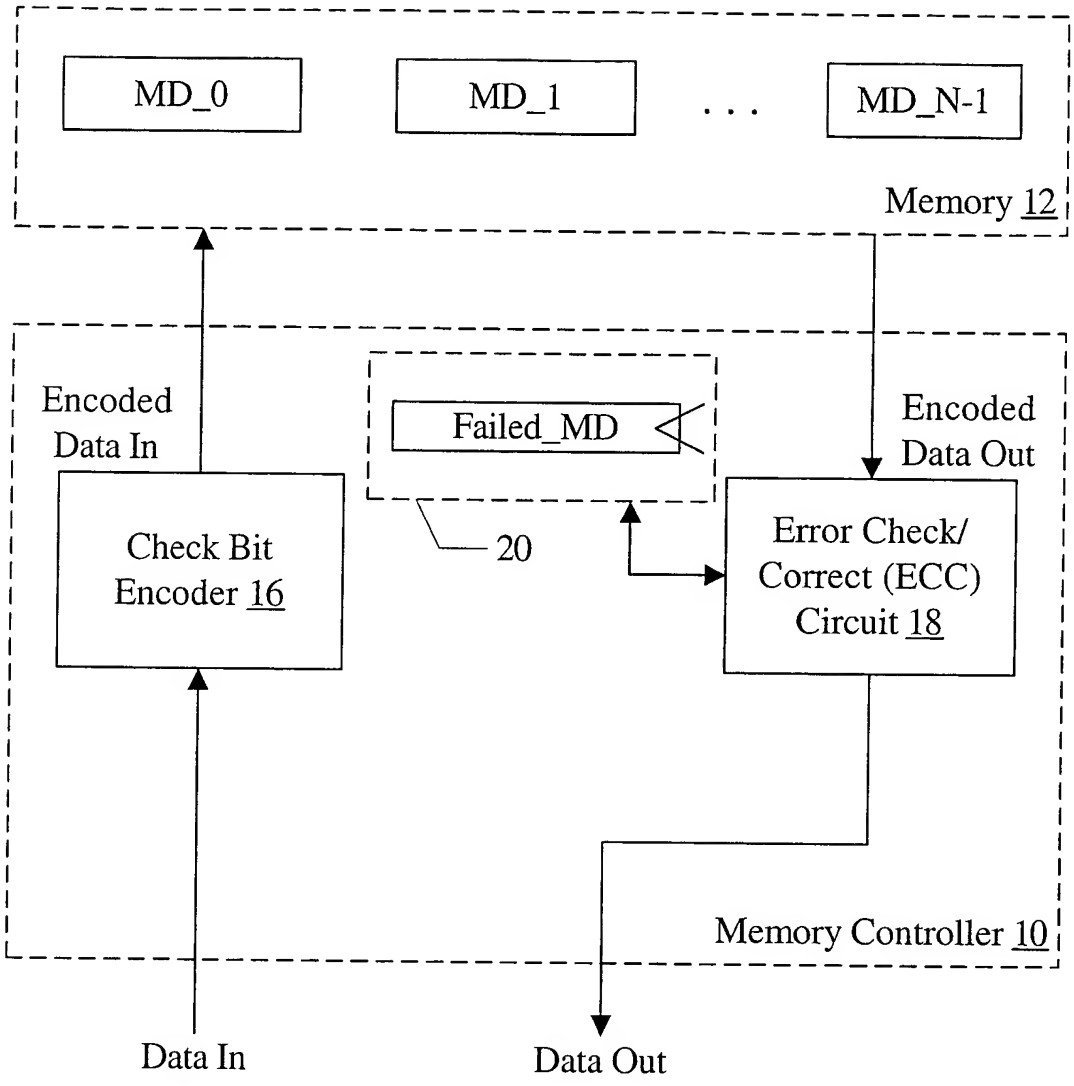
MD_0
MD_1
. . .
MD_N-1
Memory 12
Encoded
Data In
Failed_MD
Encoded
Data Out
Check Bit
Encoder 16
20
Error Check/
Correct (ECC)
Circuit 18
Memory Controller 10
Data In
Data Out

Fig. 2

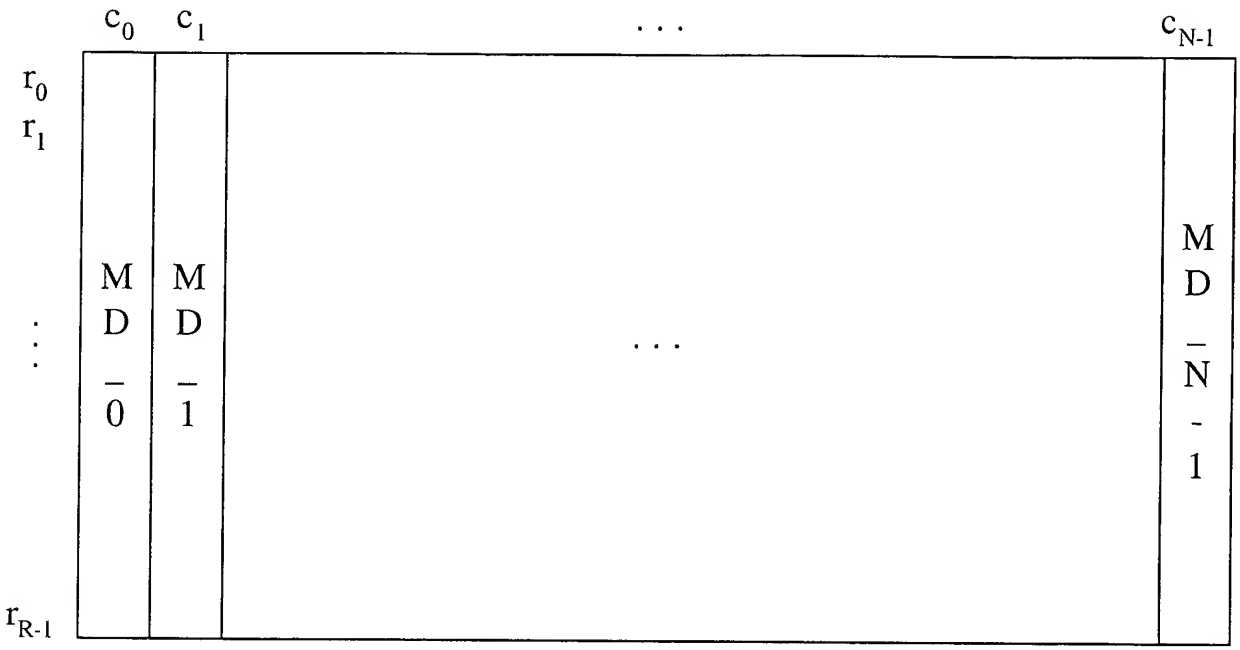

Fig. 3

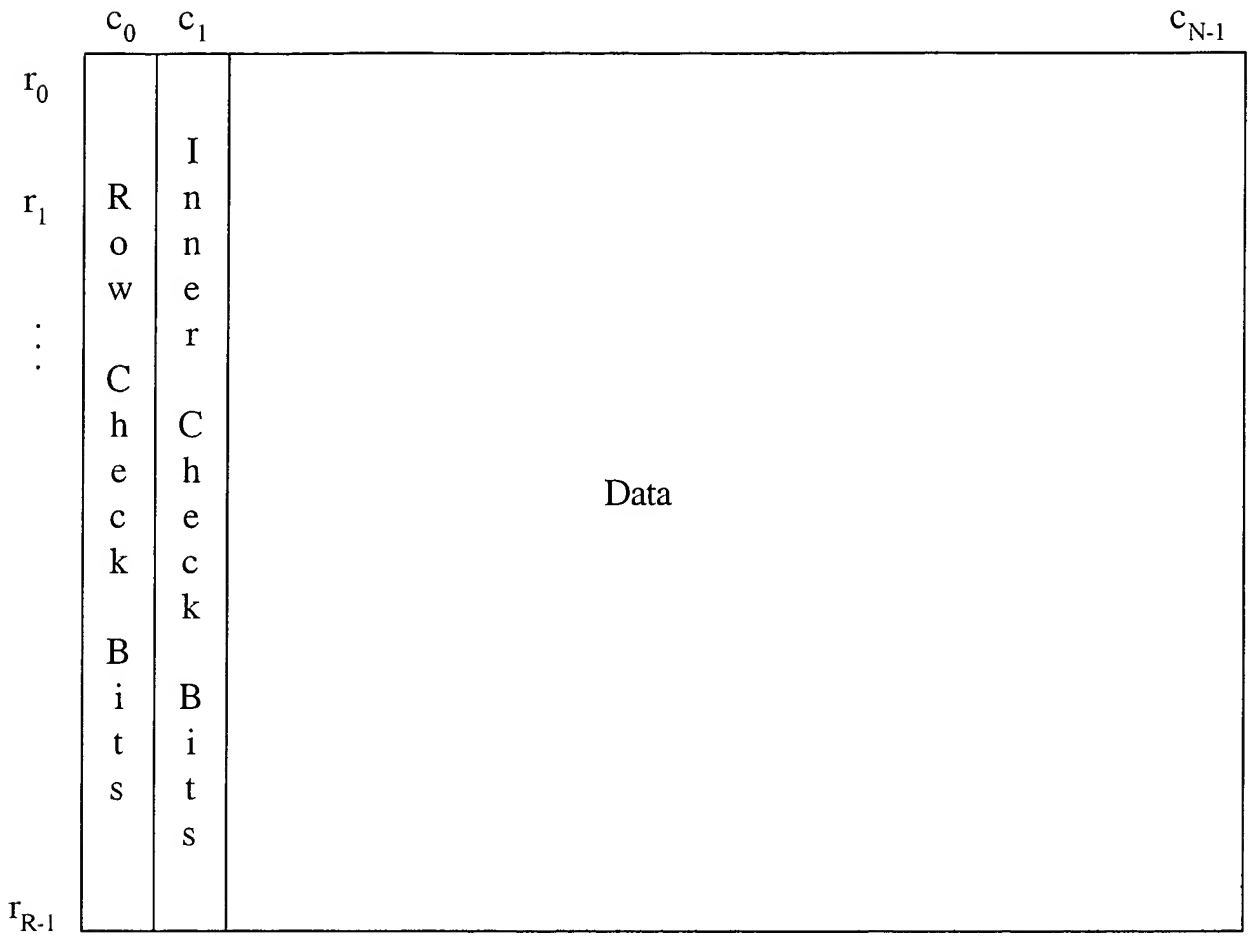

Fig. 4

$Check\_Vector(r_x, c_y) = key\_y * alpha^x$ (in $GF(2^R)$) ← 30

$row\_syn * key\_i = inner\_syn$ (in $GF(2^R)$) ← 32

$Check\_Vector(r_1, c_1)$ XOR $Check\_Vector(r_2, c_2)$ XOR $Check\_Vector(r_1, c_3)$ XOR $Check\_Vector(r_2, c_3) != 0$ ← 34

for any r_1, r_2, c_1, c_2, c_3 such that $((r_1, c_1) != (r_2, c_2)$ and $c_1 != c_3)$ or $(c_1 != c_2)$

$key\_i + key\_j != (key\_i + key\_k) * alpha^X$ $0<=X<=R-1$, i!=k, i!=j, j!=k ← 36

Fig. 5

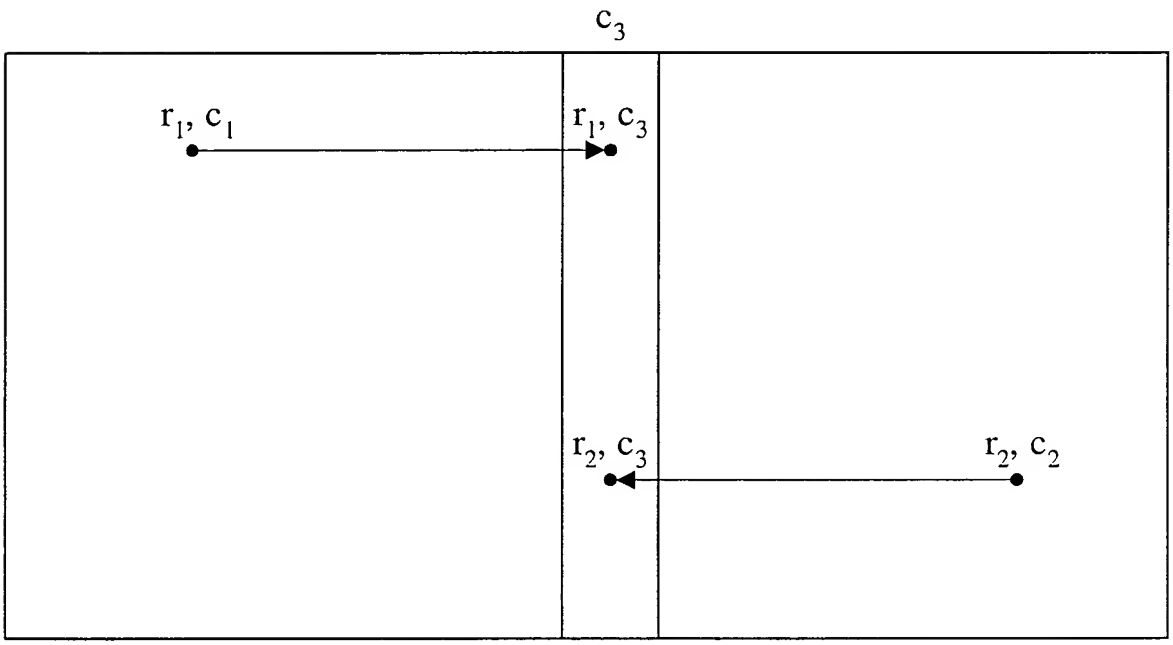

Fig. 6

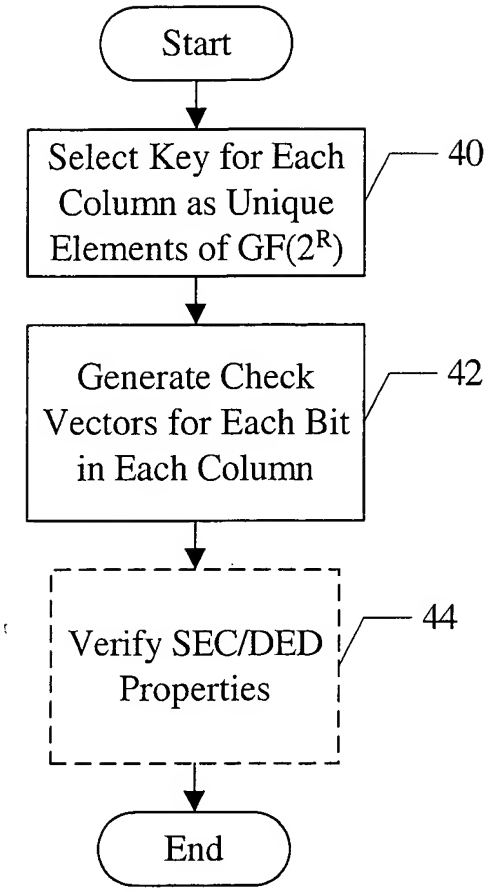
Start
Select Key for Each Column as Unique Elements of GF(2^R)
40
Generate Check Vectors for Each Bit in Each Column
42
Verify SEC/DED Properties
44
End

Fig. 7

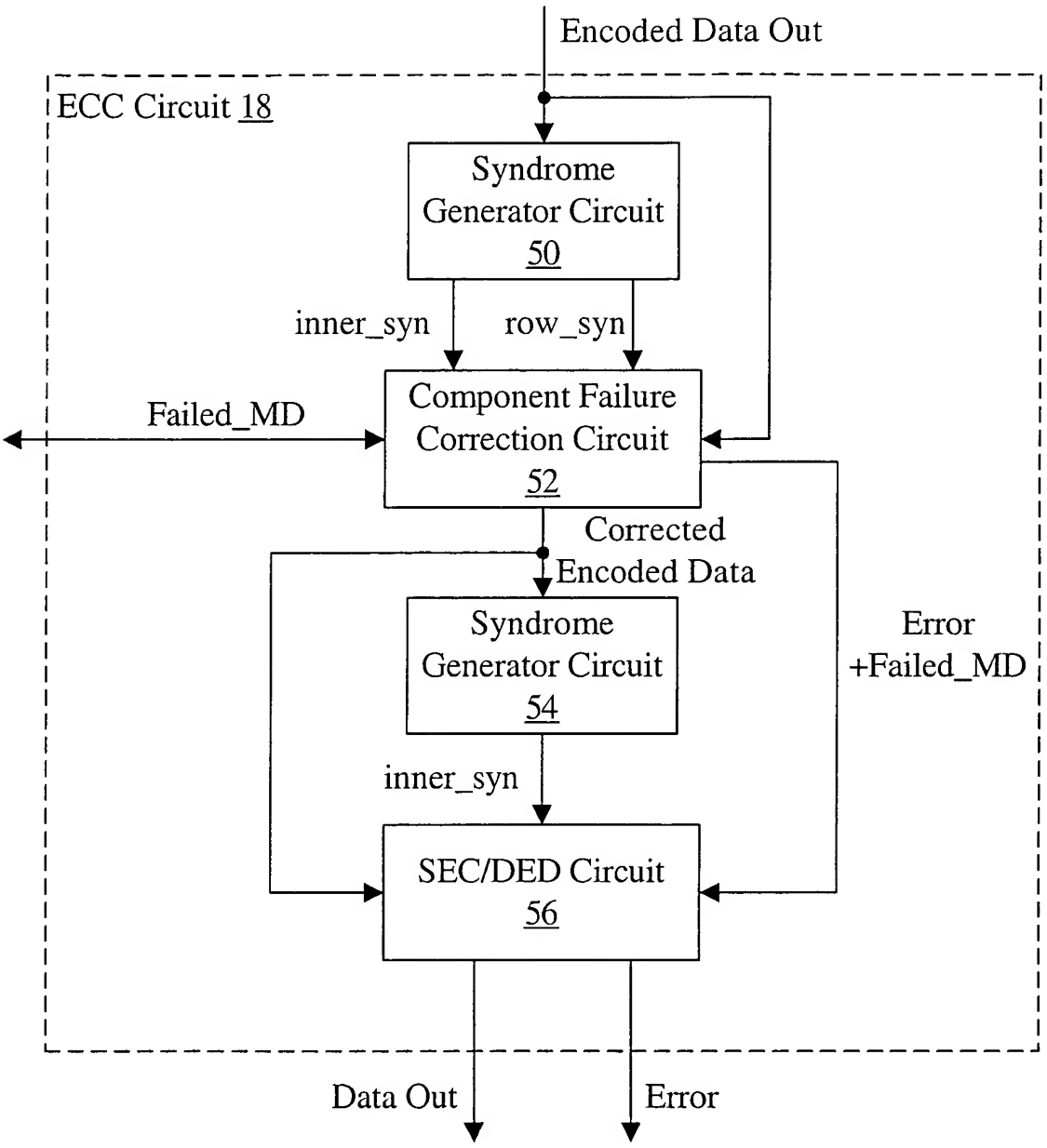
Encoded Data Out
ECC Circuit 18
Syndrome Generator Circuit 50
inner_syn
row_syn
Failed_MD
Component Failure Correction Circuit 52
Corrected Encoded Data
Syndrome Generator Circuit 54
Error +Failed_MD
inner_syn
SEC/DED Circuit 56
Data Out
Error

Fig. 8

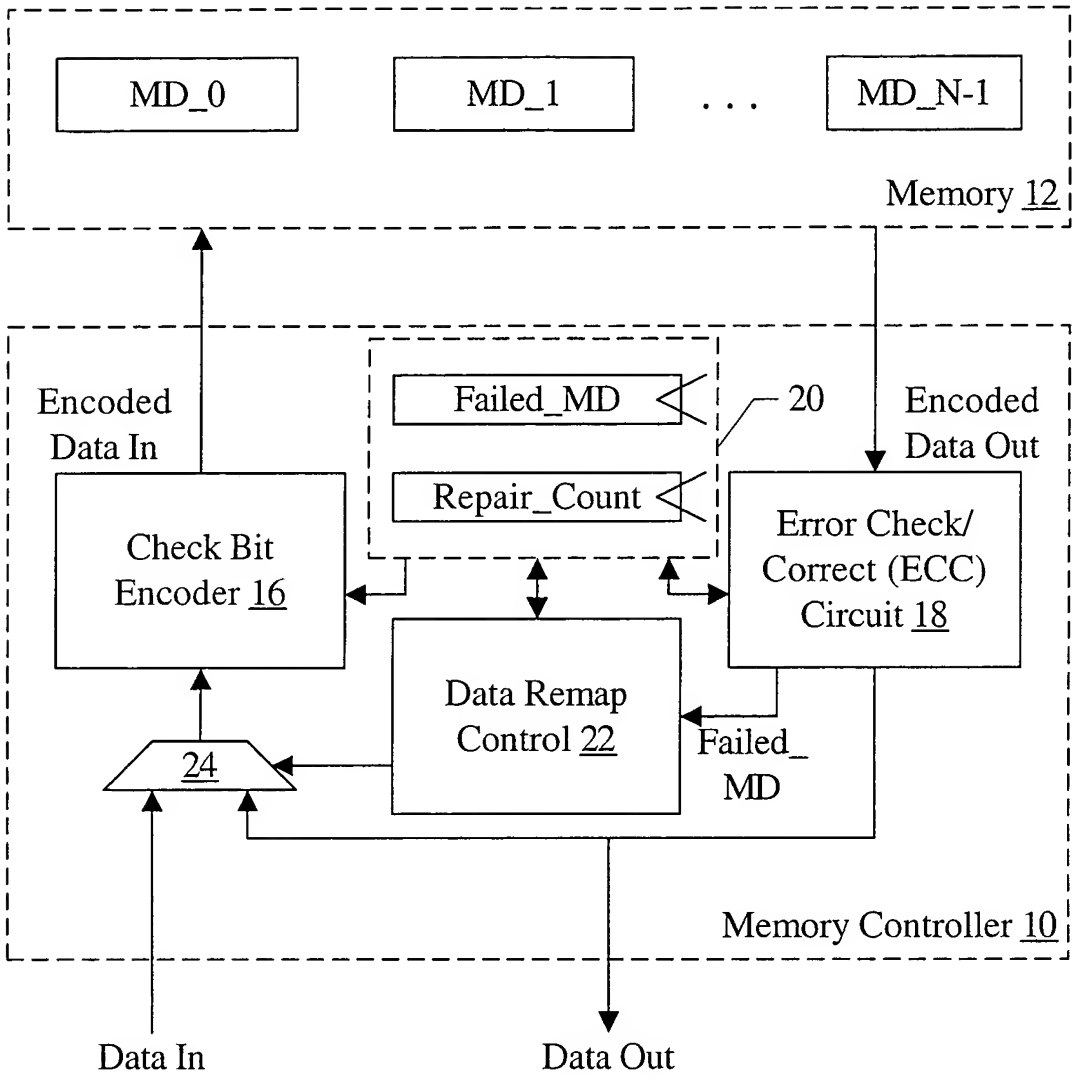
MD_0
MD_1
. . .
MD_N-1
Memory 12
Encoded
Data In
Failed_MD
20
Encoded
Data Out
Repair_Count
Check Bit
Encoder 16
Error Check/
Correct (ECC)
Circuit 18
Data Remap
Control 22
Failed_
MD
24
Memory Controller 10
Data In
Data Out

Fig. 9

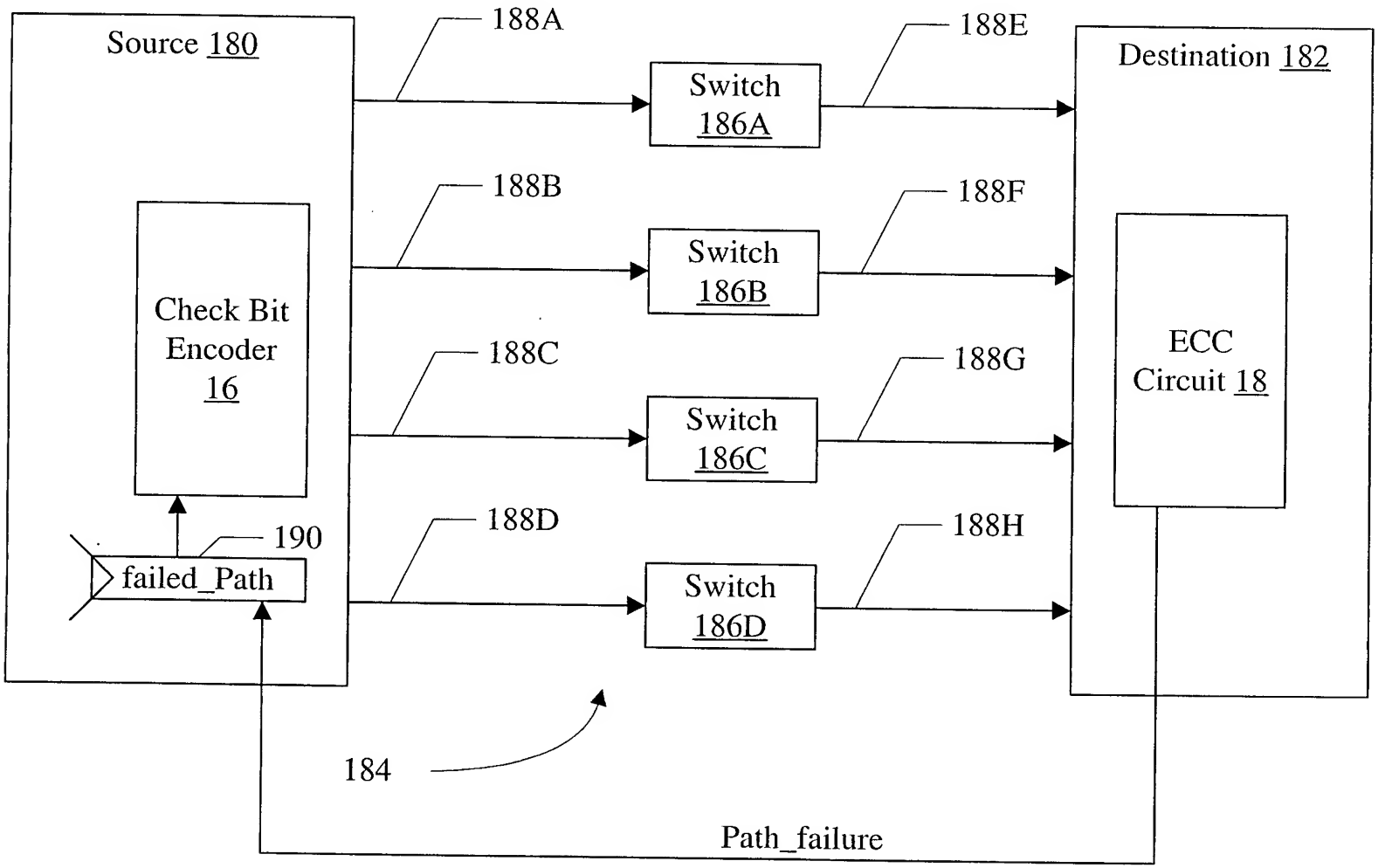
Source 180
188A
Switch 186A
188E
Destination 182
188B
Switch 186B
188F
Check Bit Encoder 16
ECC Circuit 18
188C
Switch 186C
188G
190
failed_Path
188D
Switch 186D
188H
184
Path_failure

Fig. 10

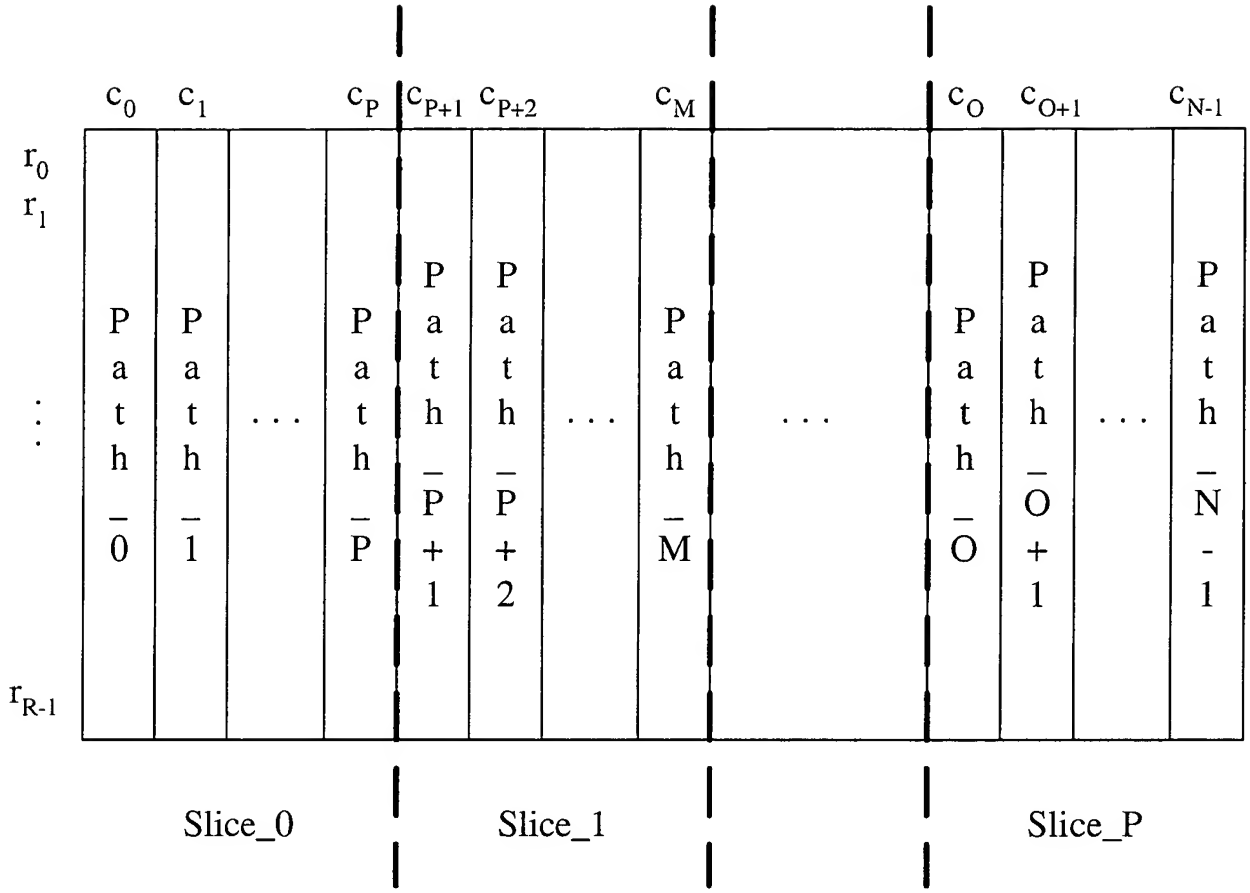
c0 c1 cP cP+1 cP+2 cM cO cO+1 cN-1
r0
r1
rR-1
Path_0
Path_1
Path_P
Path_P+1
Path_P+2
Path_M
Path_O
Path_O+1
Path_N-1
Slice_0
Slice_1
Slice_P

Fig. 11

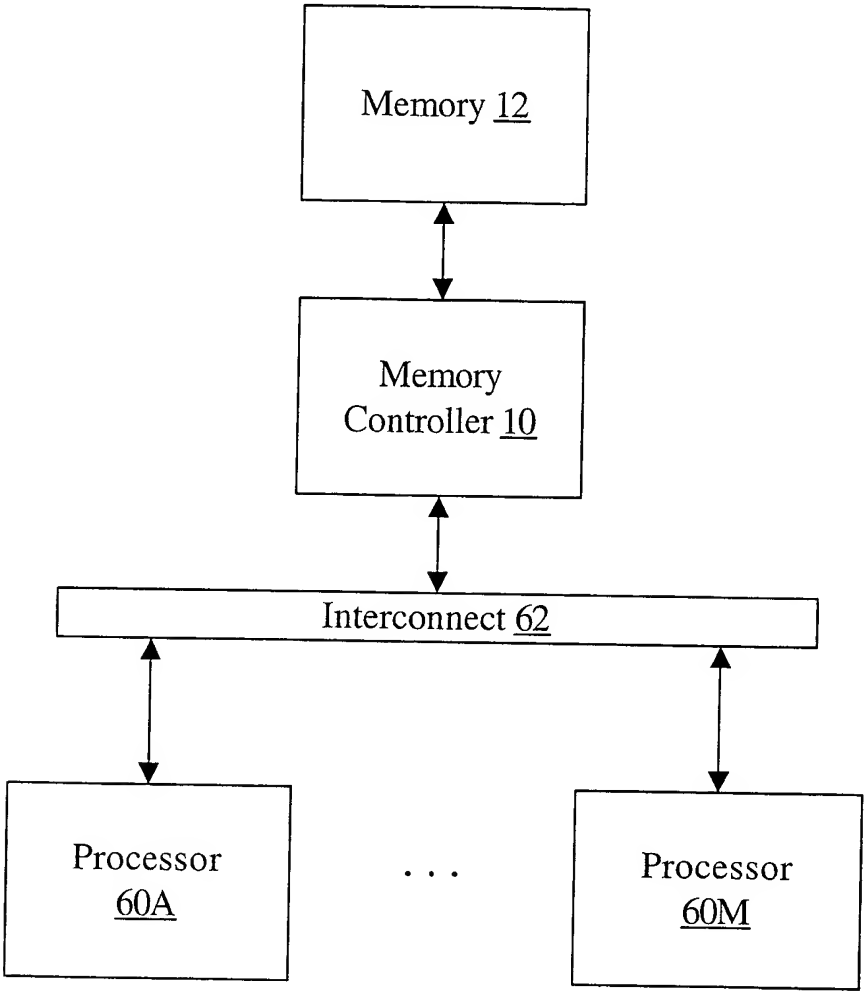
Memory 12
Memory Controller 10
Interconnect 62
Processor 60A
. . .
Processor 60M

Fig. 12